REMARKS

The claims have been amended in order to reformat the claims to delete all multiple dependencies prior to calculation of the filing fee and place the instant application in standard U.S. format.

Entry of this amendment prior to calculating the filing fee is respectfully requested.

Respectfully submitted,

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APPENDIX

- 3. (Amended) A circuit arrangement as claimed in claim $1 \cdot \frac{2}{2}$, characterized in that the signal is amplified in the pnp current mirror (16) or in the npn transistor current mirror (14).
- 4. (Amended) A circuit arrangement as claimed in <u>claim 1</u> any one of claims 1 to 3, characterized in that the high voltage source (30) supplies a voltage of the order of approximately 12 V.
- 5. (Amended) A circuit arrangement as claimed in claim 1 any one of claims 1 to 4, characterized in that the input (12) of the adapter circuit (10) is preceded by at least one supply or driver circuit (40) by which the low current (I_i) input signal can be applied to the adapter circuit (10).
- 8. (Amended) A circuit arrangement as claimed in <u>claim 1</u> any one of claims 1 to 7, characterized in that
- the npn transistor arrangement (14) is constituted as an npn current mirror and/or particularly as an NMOS current mirror (NMOS = N-channel Metal Oxide Semiconductor = N-type Metal Oxide Semiconductor); and/or
- the pnp transistor arrangement (16) is constituted as a pnp current mirror and/or particularly as a PMOS current mirror (PMOS = P-channel Metal Oxide Semiconductor = P-type Metal Oxide Semiconductor).
- 9. (Amended) A circuit arrangement as claimed in <u>claim 1</u> any one of claims 1 to 8, characterized in that the output (18) of the adapter circuit (10) precedes at least a resistor (50) for

converting the higher current (I_o) output signal into a higher voltage (U_o) output signal.

- 11. (Amended) A circuit arrangement as claimed in <u>claim 1</u> any one of claims 1 to 10, characterized in that the output (18) of the adapter circuit (10) precedes at least a SCART (= Syndicat des Constructeurs d'Appareils Radio Receteurs et Televiseurs) output (70).
- 12. (Amended) A circuit arrangement as claimed in <u>claim 1</u> any one of claims 1 to 11, characterized in that the adapter circuit (10) is multi-staged and/or more than one adapter circuit (10) is provided.
- 14. (Amended) A television, multimedia, radio or video recording device comprising at least a circuit arrangement (100) as claimed in claim 1 any one of claims 1 to 13.